MEMORY ADDRESSING

UNCLASSIFIED

RISK ASSESSMENT:

Low

SAFETY CONSIDERATIONS:

ELECTRICAL SHOCK HAZARD

ELECTROSTATIC DISCHARGE

ENVIRONMENTAL CONSIDERATIONS:

None

TERMINAL LEARNING OBJECTIVE

ACTION: Explain how the CPU addresses memory.

CONDITIONS: Given a classroom environment, an 8086 instruction set, and official OMEMS reference material.

STANDARDS: Correctly answer 14 of 20 questions on how the CPU addresses memory.

ENABLING LEARNING OBJECTIVE

ACTION: Identify the characteristics of memory addressing.

CONDITIONS: Given a classroom environment, an 8086 instruction set, and official OMEMS reference material.

STANDARDS: Correctly answer 14 of 20 questions on how the CPU addresses memory.

MEMORY ADDRESSING

The process by which the CPU accesses data in memory.

(Reading and Writing)

MEMORY ADDRESSING

The segment registers are used to divide memory into pages.

CS - Code segment

SS - Stack Segment

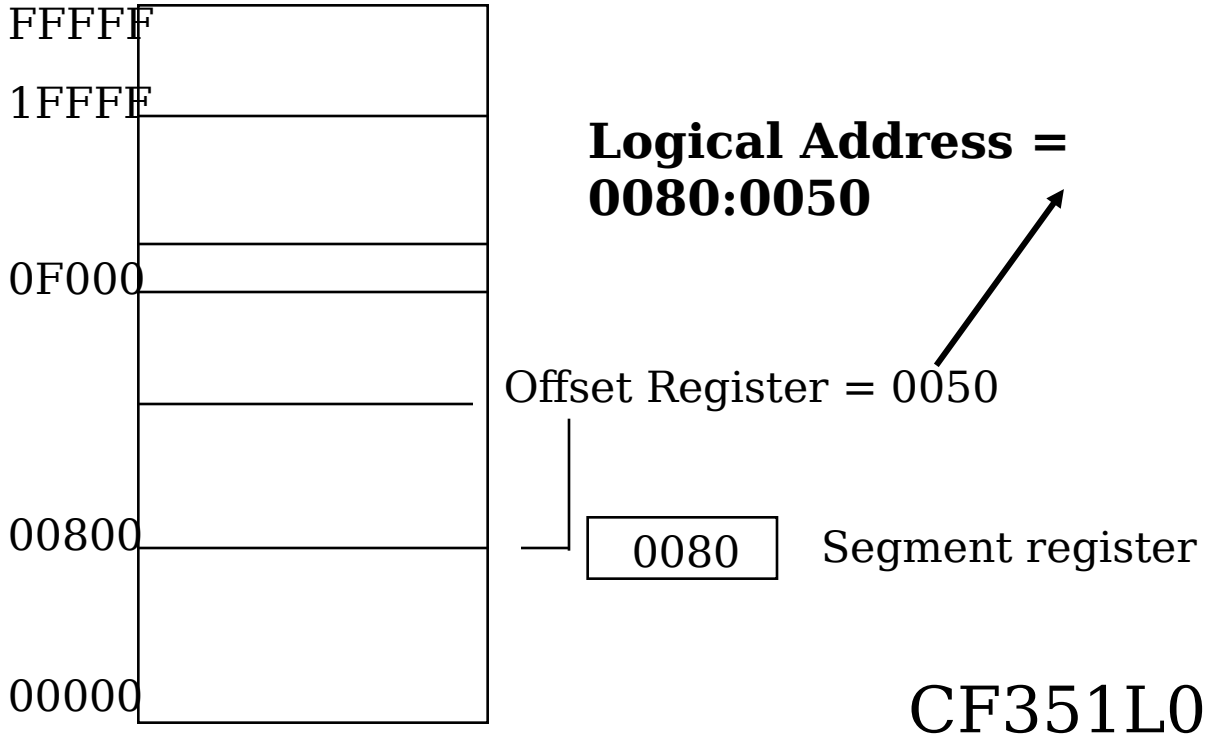
DS - Data Segment

ES - Extra Segment

The registers provide the base address.

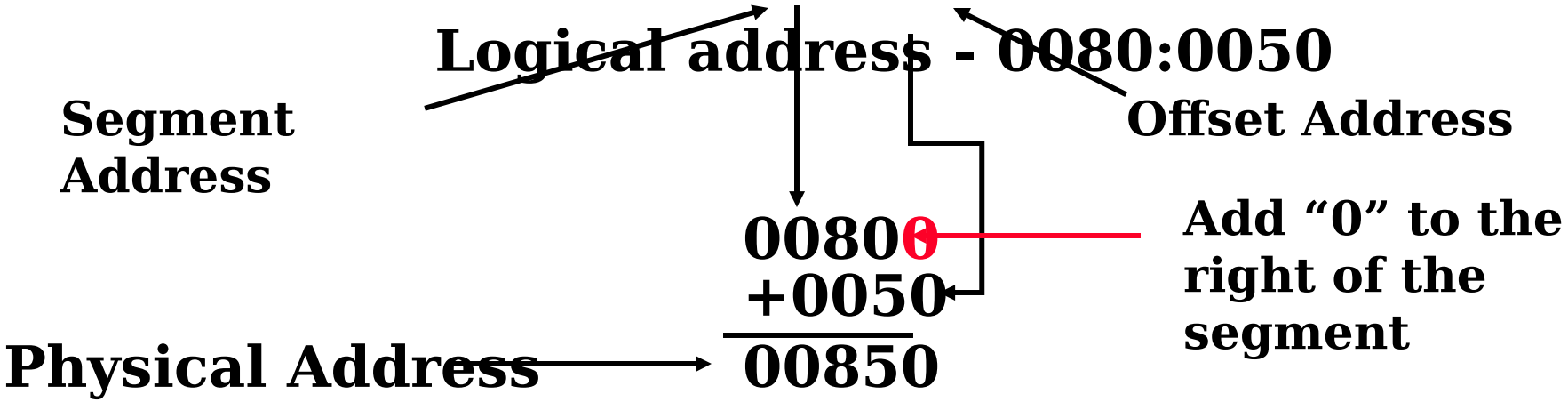
MEMORY ADDRESSING

MEMORY ADDRESSING IS PERFORMED USING A SEGMENT ADDRESS PLUS AN OFFSET ADDRESS.



MEMORY ADDRESSING

The physical address is the combination of the segment address and the offset address. This determines the actual physical location in memory.

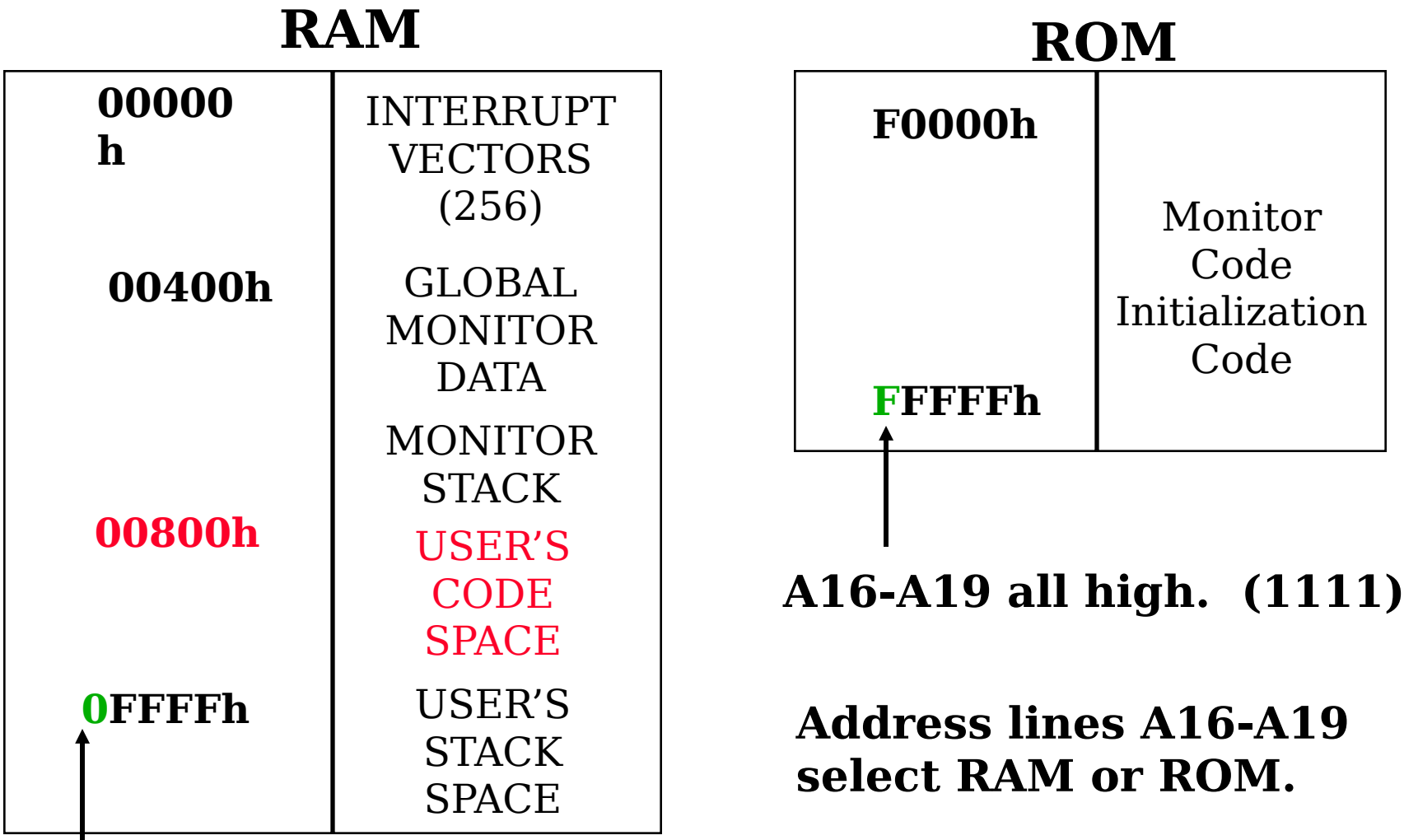


0000 0000 1000 0101 0000

The 20-bit address used by

MEMORY ADDRESSING

NIDA 500 MEMORY MAP



ENABLING LEARNING OBJECTIVE

ACTION: Identify the characteristics of registers used for memory addressing.
CONDITIONS: Given a classroom environment, an 8086 instruction set, and official OMEMS reference material.

STANDARDS: Correctly answer 14 of 20 questions on how the CPU addresses memory.

MEMORY ADDRESSING REGISTERS

MULTIPURPOSE REGISTERS

SPECIAL PURPOSE REGISTERS

SEGMENT REGISTERS

MULTIPURPOSE REGISTERS

BP - BASE POINTER

DI - DESTINATION INDEX

SI - SOURCE INDEX

Multipurpose Registers

BP - Base Pointer - Used as an offset address to access data in the stack segment.

SI - Source Index and DI - Destination Index: are used to store offset addresses of memory locations related to a segment register like the data segment.

SPECIAL-PURPOSE REGISTERS

IP = INSTRUCTION POINTER

SP = STACK POINTER

Special Purpose Registers

IP - Instruction Pointer: Contains the address of the next instruction to be executed.

SP - Stack Pointer: Addresses the next available location in the stack segment.

SEGMENT REGISTERS

Four 16-bit registers that select, at any given time, the segments of memory that are immediately addressable for code, stack, and data.

They define the beginning address of a portion of memory. The base value of an address

SEGMENT REGISTERS

CS = CODE SEGMENT

DS = DATA SEGMENT

ES = EXTRA SEGMENT

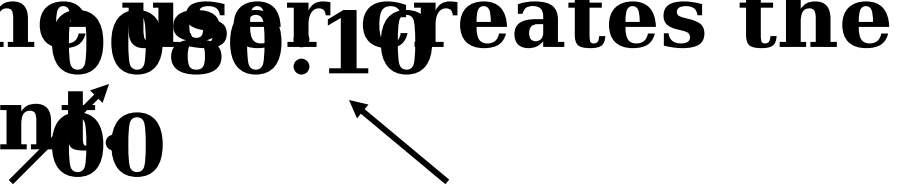
SS = STACK SEGMENT

SEGMENT REGISTER

CS - Code Segment

This section contains the starting location of a segment of memory that contains the instructions of the program.

This is where the user's program is stored. The user creates the Code Segment.



Code Segment

IP Register

SEGMENT REGISTER

DS - Data Segment

This part of memory is an area where data is stored for the program. Most operands are found in the Data Segment.

SEGMENT REGISTERS

ES - Extra Segment

This segment is used for additional storage of data. An "overflow" for the data segment.

SEGMENT REGISTERS

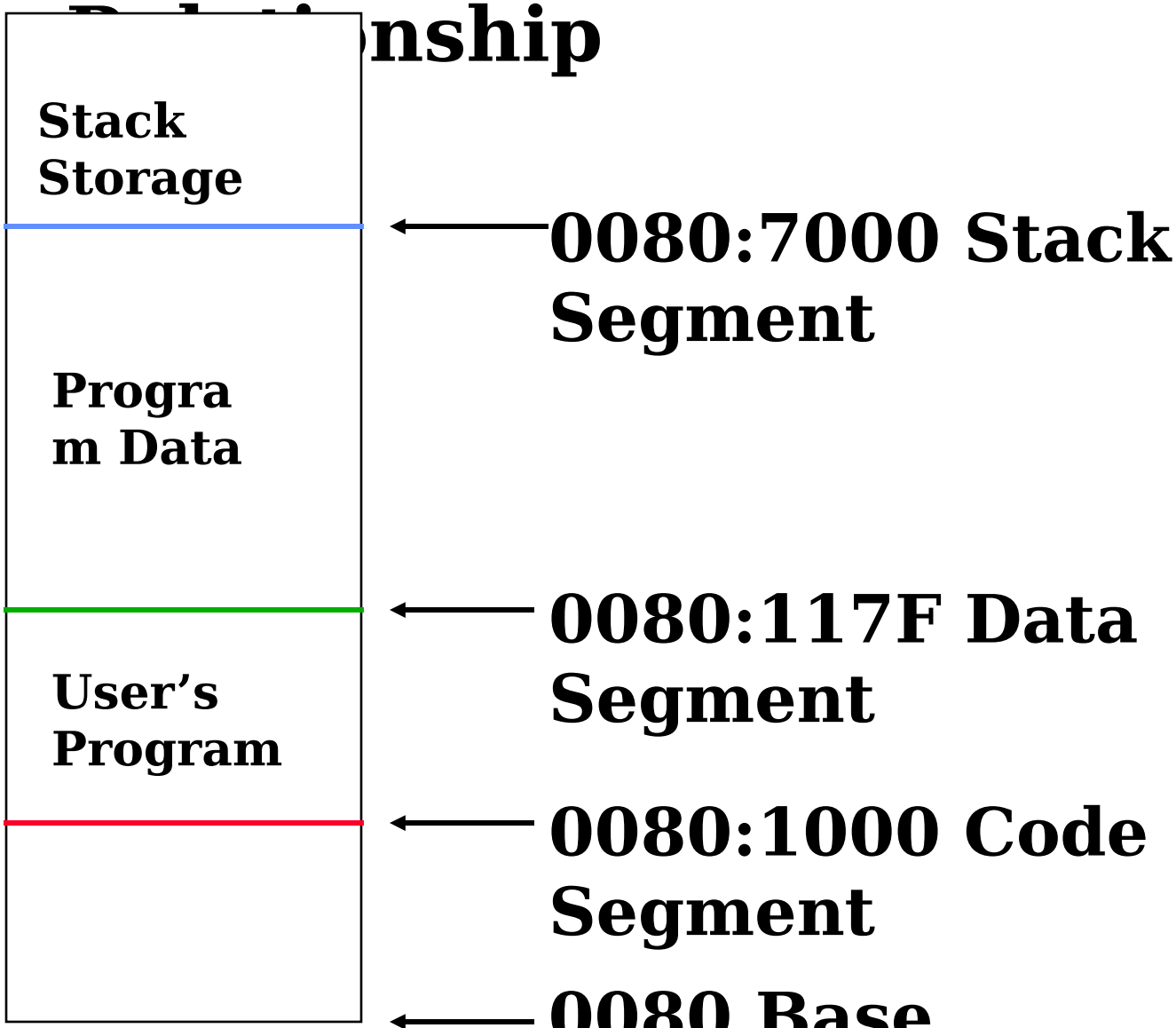
SS -Stack Segment

An area in memory that contains the status flags, instruction pointer, and other registers whenever a subroutine call occurs or a hardware or software interrupt occurs.

Stack Segment

Stack Pointer

Segment Register Relationship



ENABLING LEARNING OBJECTIVE

ACTION: Identify memory addressing modes.

CONDITIONS: Given a classroom environment, an 8086 instruction set, and official OMEMS reference material.

STANDARDS: Correctly answer 14 of 20 questions on how the CPU addresses memory.

ADDRESSING MODES

Immediate Operand Addressing Mode

Register Operand Addressing Mode

Direct Addressing Mode

Based Addressing Mode

Register Indirect Addressing Mode

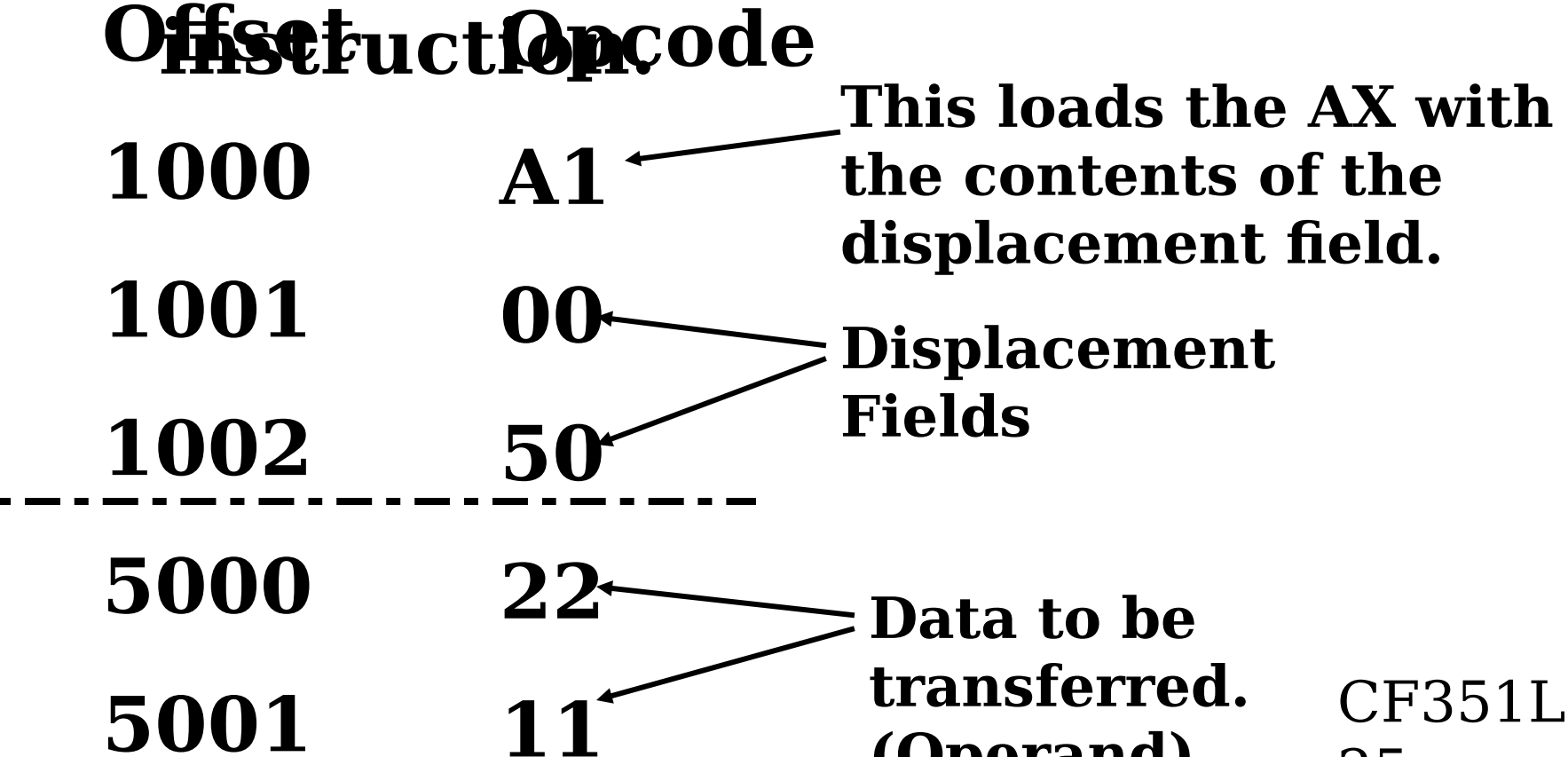
Indexed Addressing Mode

Based Indexed Addressing Mode

Based Indexed with Displacement Addressing Mode

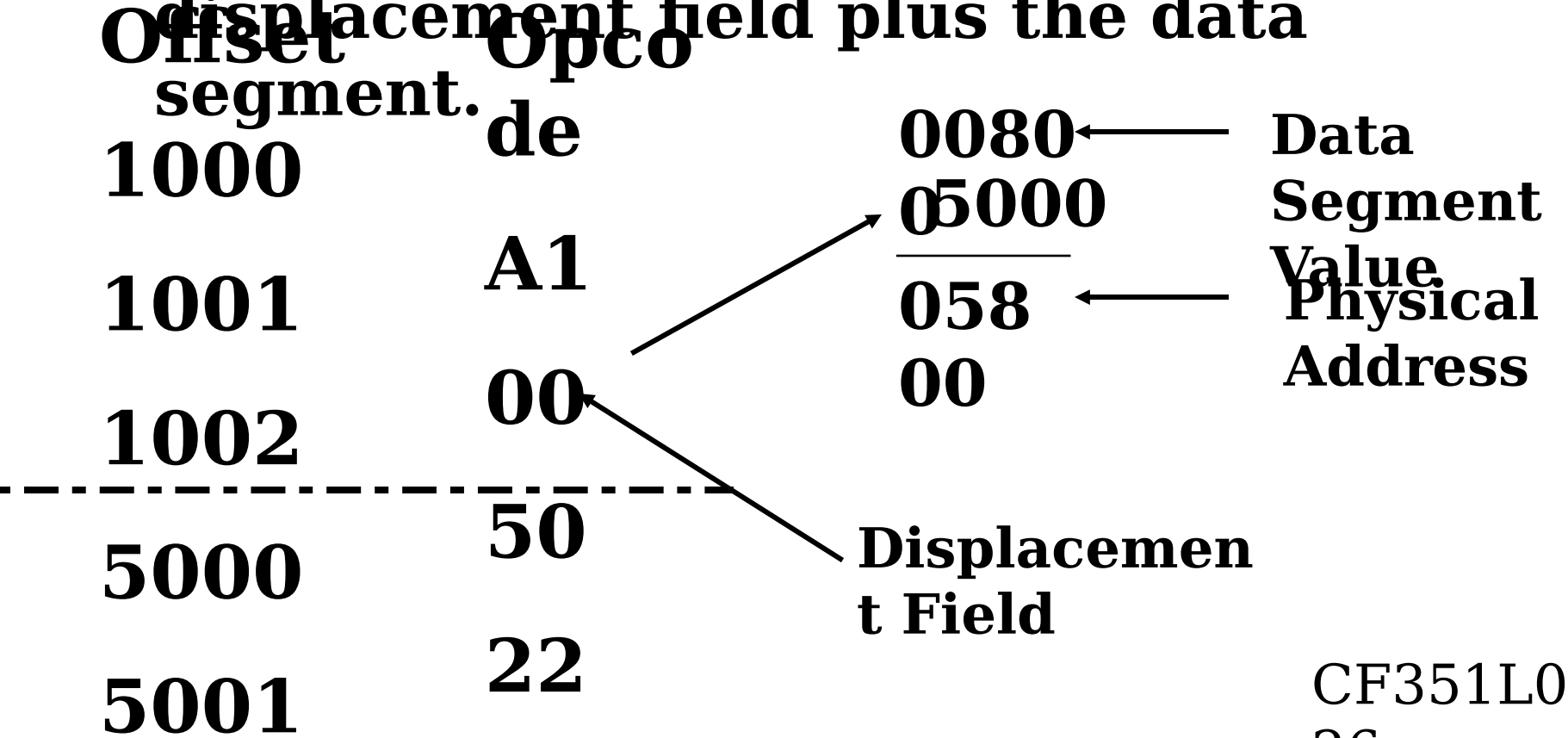
Direct Addressing Mode

The effective address of the operand is contained in the displacement fields of the instruction.



Direct Addressing Mode Physical Address

The physical address of the operand is derived by adding the displacement field plus the data segment.



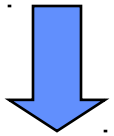
Register Indirect Addressing Mode

The effective address of the operand is in the base register (BX or BP) or index (SI or DI) register.

Offset	Opcode
1000	8B
1001	04
5000	44
5001	33

Move the contents of location specified by the SI register to the AX register.

AX: 0000
SI: 5000



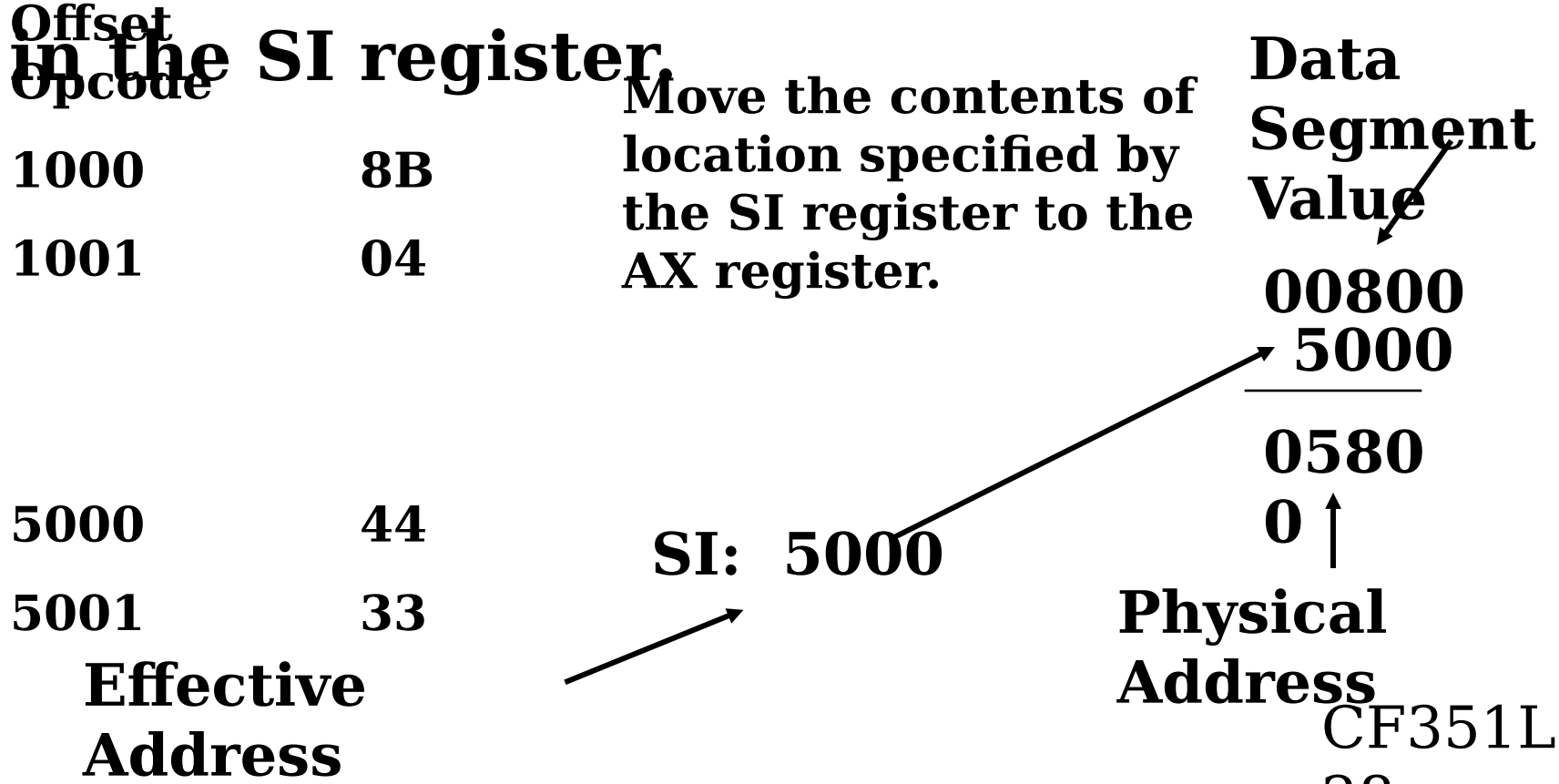
AX: 3344
SI: 5000

SI: 5000

Effective Address

Register Indirect Addressing Mode Physical Address

The physical address of the operand is derived by adding the data segment value to the effective address contained in the SI register.



Based Indexed Addressing

The effective address of the operand is derived by adding the contents of the base register (BX or BP) and the index register (SI or DI).

Offset	Opcode
1000	8B
1001	00
5050	44
5051	33

Move the contents of location specified by the SI and the BX to the AX register.

SI: 5000

BX: 0050

5050

Effective Address

AX: 0000

BX: 0050

SI: 5000

AX: 3344

BX: 0050

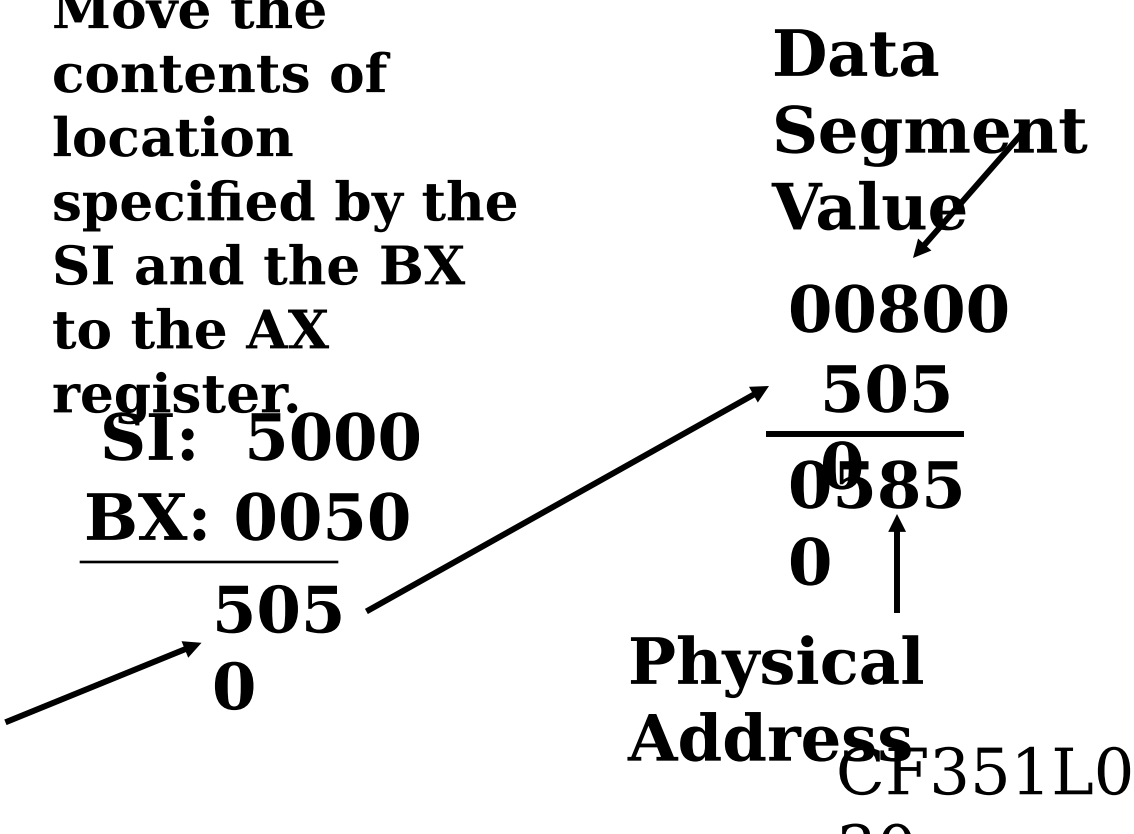
SI: 5000

Based Index Addressing Mode Physical Address

The physical address of the operand is derived by adding the data segment value and the effective address.

Offset	Opcode
1000	8B
1001	00
5050	44
5051	33

Move the contents of location specified by the SI and the BX to the AX register.



Based Index Addressing With Displacer

The effective address of the operand is derived by adding a displacement, whose value is specified in the instruction, to the value in the base register (BX or BP). This is then added to the contents of an index register (SI or DI).

Offset	Opcode
1000	8B
1001	40
1002	50
5050	44
5051	33

Move the contents of location specified by the SI, BX, and displacement value to the AX register.

SI: 2B00
BX: 2500
Disp: 50

505
0

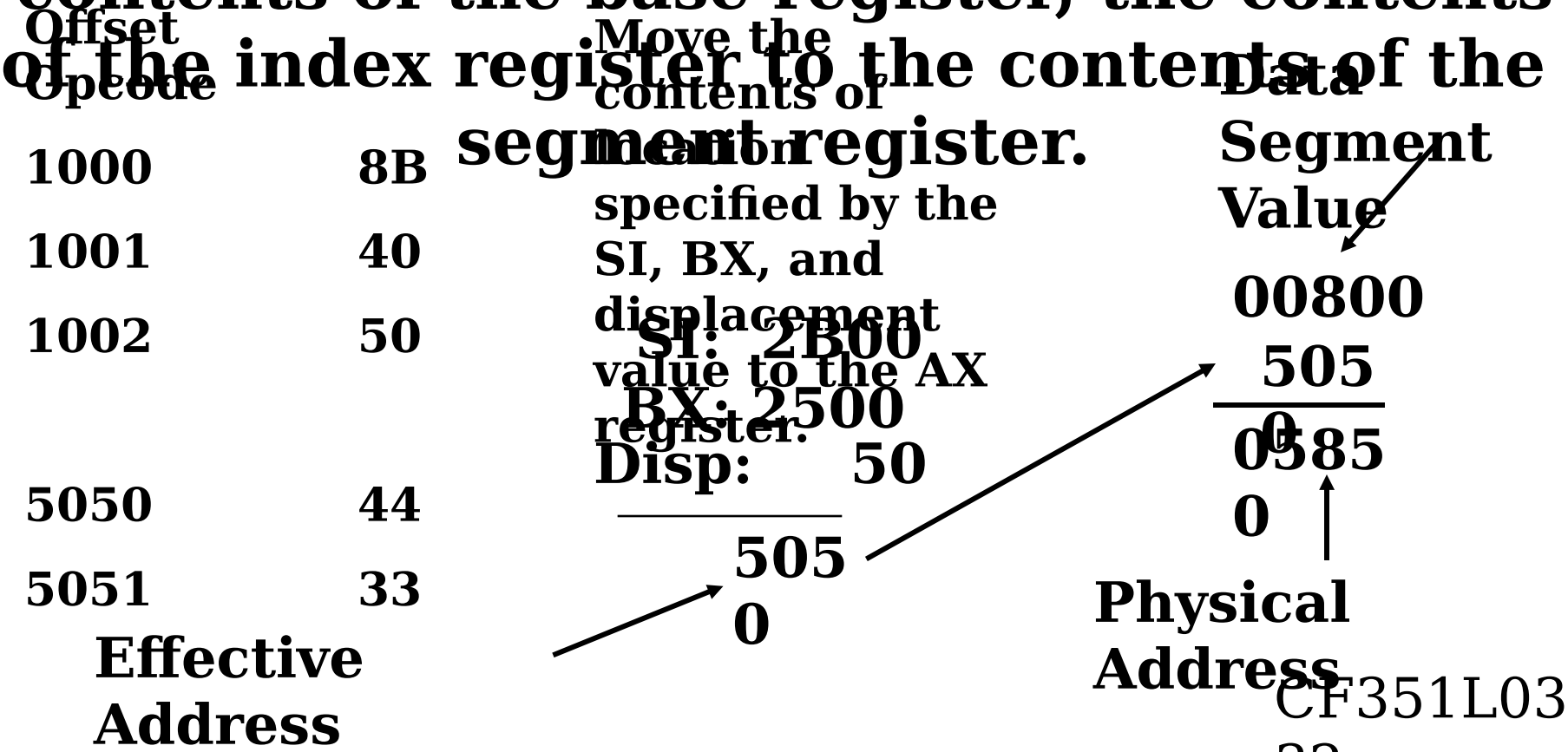
Effective Address

AX:
0000
SI:
2B00
BX:
2500
Disp:
50

AX:

Based Index Addressing With Displacement Mode Physical Address

The physical address of the operand is derived by adding the displacement, the contents of the base register, the contents of the index register to the contents of the segment register.



ENABLING LEARNING OBJECTIVE

ACTION: Utilize the different memory addressing.

CONDITIONS: Given a classroom environment, an 8086 instruction set, and official OMEMS reference material.

STANDARDS: Correctly answer 14 of 20 questions on how the CPU addresses memory.

Write a program that will transfer the word FFFF from a specified memory location to the AX register using:

Direct Addressing Mode

Register Indirect Addressing Mode

Based Plus Index Addressing Mode

Based Index with Displacement Addressing Mode (8 bit displacement)

Memory Addressing Practical Exercise

For each of the modes the memory location to be used is:

0080:4A4B and 0080:4A4C. Manually load these locations with FFFF.

Each mode used must move FFFF from the above memory location to the AX register.